

January 11, 2004

Case No.: FR 000130 (7790/194)

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CLAIM AMENDMENTS

A listing of the entire set of pending claims 1-9 is submitted herewith per 37 C.F.R. §1.121. This listing of pending claims 1-9 will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A data-processing system, comprising:
a microprocessor [PRC];
a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and
a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].
2. (Previously Presented) The data-processing system as claimed in claim 1, wherein said electronic module [MOD] is a Subscriber Identity Module card.
3. (Previously Presented) The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.
4. (Previously Presented) The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] includes:
a switch [SWHMP, SWHPM];
a right shift register [RXMP, RYPM] electrically connected to said switch;
and
a left shift register [RYMP, RXPM] electrically connected to said switch.

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5. (Previously Presented) A terminal, comprising:
a microprocessor [PRC];
a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and
a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].
6. (Previously Presented) The terminal as claimed in claim 5, wherein said electronic module [MOD] is a Subscriber Identity Module card.
7. (Presently Presented) The terminal as claimed in claim 5, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.
8. (Previously Presented) The terminals as claimed in claim 5, wherein said hardware circuit [HARD] includes:
a switch [SWHMP, SWHPM];
a right shift register [RXMP, RYPM] electrically connected to said switch;
and
a left shift register [RYMP, RXPM] electrically connected to said switch.
9. (Previously Presented) A data-processing system, comprising:
a hardware circuit [HARD];
a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]; and
wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal.